UNIVERSAL COUNTER TIMER

Type SA.7535

Operating & Maintenance Manual

Technical Handbooks Department

RACAL ELECTRONICS PTY. LIMITED
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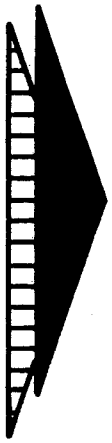
THE NEXT TWO PAGES

concern all users of electrical equipment from a different point of view

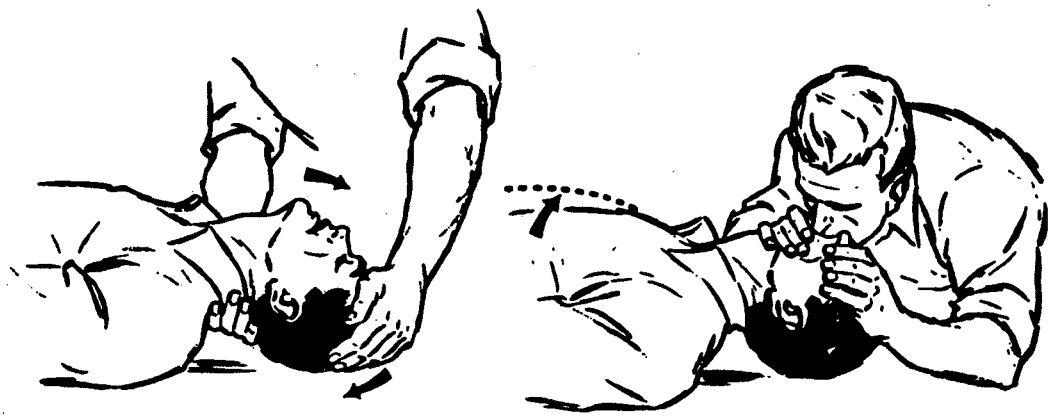
●

read carefully .....it

COULD AFFECT YOU



FIRST AID in case of Electric Shock



ON BACK : TILT HEAD BACK AS FAR AS POSSIBLE : RAISE THE JAW.

PINCH VICTIM'S NOSE : KEEP HEAD BACK : BLOW UNTIL THE CHEST RISES.

RESCUE BREATHING

1. LAY VICTIM ON HIS BACK.
2. CLEAR HIS MOUTH AND THROAT.
3. TILT HIS HEAD BACK AS FAR AS POSSIBLE AND RAISE HIS JAW.
4. PINCH HIS NOSTRILS.
5. TAKE A DEEP BREATH.
6. COVER HIS MOUTH WITH YOURS AND BLOW, WATCHING HIS CHEST RISE. (FORCEFULLY INTO ADULTS AND GENTLY INTO CHILDREN).
7. MOVE YOUR FACE AWAY FOR HIM TO BREATHE OUT, WATCH HIS CHEST FALL.
8. REPEAT YOUR FIRST FIVE TO TEN BREATHS AT A RAPID RATE. THEREAFTER TAKE ONE BREATH EVERY THREE TO FIVE SECONDS.
9. KEEP HIS HEAD BACK AS FAR AS POSSIBLE ALL THE TIME.

Have someone else send for a Doctor

Keep patient warm and loosen his clothing

DO NOT Give liquids until patient is conscious

DANGER HIGH VOLTAGES

ADJUSTMENTS EXERCISE GREAT CARE

SERVICING SWITCH OFF

Although every reasonable precaution has been observed in design to safeguard operating personnel this warning is ... VITAL !

now . . .

proceed

with

CAUTION

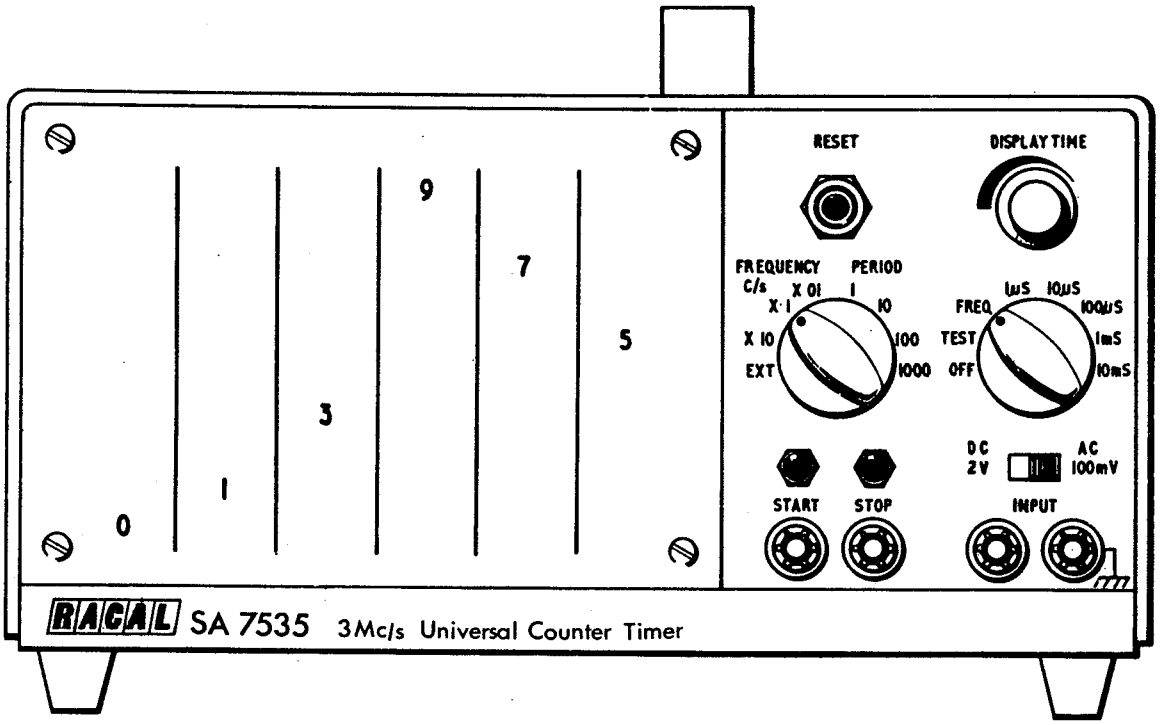
HANDBOOK CHANGE INFORMATION

At RACAL, we continually strive to keep up with the latest electronic developments by adding circuit and component improvements to our equipments.

Sometimes, due to printing and despatch requirements, we are unable to incorporate these changes immediately into printed handbooks. Hence, your handbook may contain new change information on following pages.

The user is recommended to hand-amend this handbook, as soon as possible, in accordance with the corrections, if any, which follow this sheet.

NOTES



Universal Counter-Timer Type SA7535

UNIVERSAL COUNTER-TIMER

TYPE SA.7535

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LIST OF ILLUSTRATIONS

TECHNICAL SPECIFICATION

Frequency Measurement

Range :	a.c. coupled 10 c/s to 3 Mc/s. d.c. coupled 0 to 3 Mc/s.
Counting Periods :	0.1, 1 and 10 seconds.
Sensitivity :	
a.c. coupled	Minimum ± 140mV excursion about mean level (equivalent to 100mV r.m.s. sinewave). Maximum a.c. component 100V r.m.s. at 10 c/s, 250V r.m.s. at 50 c/s and above. Maximum d.c. component 400V.
d.c. coupled	Minimum ±2V excursion about zero volts. Maximum 150V r.m.s.
Input Impedance :	100kΩ in parallel with 40pF (greater than 50k on d.c.).
Accuracy :	±1 count ± internal crystal stability.

Period Measurement

Range :	10^{-4} c/s to 30 kc/s.
Sensitivity :	As for Frequency Measurement.
Input Impedance :	100kΩ in parallel with 40pF.
Measurement Periods :	1, 10, 100 and 1000 cycles of the unknown input.
Clock Pulses :	1μS, 10μS, 100μS, 1 mS and 10 mS.
Accuracy : (At an input level of 1V r.m.s.)	Period 1 : ±0.3% ± clock pulse accuracy ±1 count. Period 10 : ±0.03% ± clock pulse accuracy ±1 count. Period 100 : ±0.003% ± clock pulse accuracy ±1 count. Period 1000 : ±0.0003% ± clock pulse accuracy ±1 count.

SA. 7535

Time-Interval Measurement

Time Range :	2μS to 10^4 seconds.
Clock Pulses :	As for Period Measurement.
Input Mode :	(a) Two-line start-stop by external pulses. (b) Two-line start-stop by pushbuttons on front panel.
Input Characteristics :	8V to 15V positive pulses with minimum pulse width of 0.5μS at half height and a maximum rise-time of 0.2μS.

General Information

Display :	6 digit display, illuminated numbers set in vertical scales, display switched off during count period.
Display Time :	0.5 to 10 seconds approximately or infinite.
Reset :	Automatic, manual or by external positive signal pulse of 6V to 15V with a minimum width of 1μS and maximum rise-time of 5μS.
Operating Temperature Range :	0°C to $+45^{\circ}$C external ambient.
Internal Frequency Standard :	1 Mc/s oven-controlled crystal oscillator with a stability of ± 1 part in 10^6 over ambient operating temperature range.
External Standard :	1 Mc/s $\pm 1\%$ at a level from 1.0V r.m.s. to 20V r.m.s. Input impedance is 10 kilohms in parallel with 10pF.
Auxiliary Outputs :	(a) 10 lines at high impedance from each indicating decade for operation of external digital recorders. (b) Control lines including 'print command' signals. (c) Standard frequencies of 10^2, 10^3, 10^4, 10^5 and 10^6 c/s available at a socket on the rear of the instrument.

Power Supply :	Mains :	115, 200, 220 and 240 volts a.c. (±10%) 45-60 c/s, single phase, 25 watts.
	Battery :	(a) +12 volts ±1 volt with respect to chassis, load current 0.16 amp.
		(b) -12 volts ±1 volt with respect to chassis, load current 0.9 amp.
		Note that lamp brilliance is reduced on battery operation.

Mechanical

Dimensions :	Height	Width	Depth
	6.75	11.3	7.25 in.
	17.5	29	18.5 cm.

Weight : 9 lb. (4 kg) approximately.

SECTION 1

OPERATING AND DESCRIPTION

CONTENTS

CHAPTER 1

GENERAL DESCRIPTION

Introduction

1. The Universal Counter-Timer Type SA. 7535 is a portable instrument designed to make frequency, period and time-interval measurements up to a maximum frequency of 3 Mc/s. The accuracy of any measurement is determined by an internal crystal oscillator with a stability of ± 1 part in 10^6.

2. Solid state techniques are employed throughout the instrument; all circuitry with the exception of a small number of components associated with the power supplies are mounted on printed wiring boards. Measurements are displayed on six vertical decades by 'one-out-of-ten' filament bulbs on the front of the unit.

3. The instrument may be gated by externally applied positive pulses enabling time-intervals to be measured with an accuracy of ± 1 microsecond, or by the operation of the pushbutton switches on the front panel.

4. Outputs (1 out of 10) are available for the direct operation of digital recorders, e.g. a Racal 10-Way Serializer Type SA. 538B and any 24 volt Addo-X Solenoid Printer, to give a permanent printed digital record.

5. The instrument is designed to operate either from 115 volts and 200-240 volts, 45-60 c/s mains supply or from external 12 volt batteries.

CHAPTER 2

OPERATING INSTRUCTIONS

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ILLUSTRATIONS

CHAPTER 2

OPERATING INSTRUCTIONS

IMPORTANT NOTE : Before any tests or measurements are carried out, ensure that the INT./EXT. STANDARD switch, on the rear, is set to INT. (See paras. 26 and 27.)

POWER SUPPLY

Mains Operation

1. The instrument may be operated from a mains supply of either 110-120 volts or 190-250 volts at 45-60 c/s. Before connecting the instrument to the mains supply, check that the voltage selector panel is correctly set and that the correct fuses are inserted for the mains voltage in use. Ensure also that the MAINS/BATTERY switch, at the rear of the unit, is in the MAINS position.

2. For mains voltages between :-

110 to 120 volts, use 115-volt tap and 2 amp fuses.

190 to 210 volts, use 200-volt tap and 1 amp fuses.

210 to 230 volts, use 220-volt tap and 1 amp fuses.

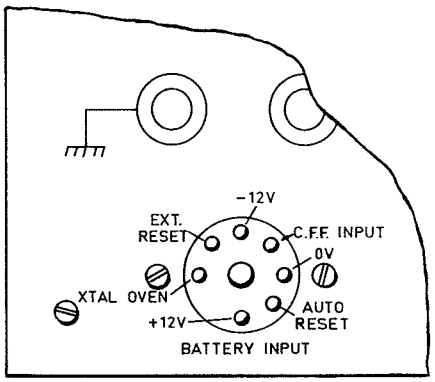
230 to 250 volts, use 240-volt tap and 1 amp fuses.

Battery Operation

CAUTION : It is important that the batteries are correctly connected otherwise serious damage will occur.

3. Battery operation of the instrument requires two 12-volt batteries. The BATTERY-MAINS switch SC, located at the rear of the unit, must be set to the BATTERY position. Connections to the battery supply are made via a socket at the rear of the unit. The figure overleaf shows a mating view of the socket and indicates the polarities to be observed.

4. The display bulbs will be somewhat dimmer when operating from a battery supply than when working from a mains supply.



Battery Supply Connections SA7535 Fig. 2-1

5. The OFF position of the Function switch is in-operative when operating from a battery supply and therefore, to switch the instrument off, the batteries must be disconnected.

INSTRUMENT CHECK

6. This check should be carried out before using the instrument.

(1) Check that the AC-DC switch is in the AC position and that the INT-EXT STANDARD switch at the rear of the unit is in the INT position.

(2) Set the Count switch to TEST.

(3) Set the Function switch to FREQUENCY X10.

(4) The displayed count should be 100000, 099999 or 100001.

(5) Set the Function switch to FREQUENCY X1 and FREQUENCY X0. 1.

(6) The displayed count should be 000000, 999999 or 000001.

NOTE 1 : The instrument test procedure cannot be carried out with the Function switch in any of the PERIOD positions hence any displayed count should be ignored.

NOTE 2 : It is essential that the AC-DC switch is not operated whilst an input signal is applied to the unit. See paras. 26 and 27 for the operation of the INT-EXT STANDARD switch.

FREQUENCY MEASUREMENT

7. (1) Set the Count switch to FREQUENCY.

(2) Switch to either AC or DC depending on the signal under test. (See paras. 33 to 37.)

(3) Connect the unknown frequency to the INPUT (Red is line : Black is chassis and earth) terminals.

(4) For a.c. operation, ensure that the signal under measurement is greater than 70 millivolts and less than 100 volts r.m.s. at 10 to 50 c/s; or less than 250 volts r.m.s. for 50 c/s and above. For d.c. operation, the signal amplitude must be greater than 2 volts and less than 150 volts r.m.s. about earth reference.

(5) Set the DISPLAY TIME control as required. If an 'infinite' display time is selected, a new counting period will not commence until the instrument is manually or externally reset. (See paras. 38 to 40.)

(6) Set the Function switch to FREQUENCY X10.

(7) The displayed count multiplied by 10 indicates the frequency in cycles per second, to the nearest 10 c.p.s.

(8) Set the Function switch to FREQUENCY X1.

(9) The displayed count is a direct reading in cycles per second of the signal under measurement.

(10) Set the Function switch to FREQUENCY X0.1.

(11) The displayed count divided by 10 gives the frequency under measurement to the nearest 1/10 of a cycle per second.

NOTE 1 : The most significant digits may overspill the display in the FREQUENCY X1 and FREQUENCY X0.1 positions, therefore, a note of the display in the FREQUENCY X10 position should always be made.

NOTE 2 : As per para. 6 opposite.

8. When making measurements below 10 kc/s, greater accuracy is obtained by making PERIOD measurements and calculating the frequency. (See paras. 9 to 12.)

NOTE 1 : It is important that when making frequency measurements the peak amplitude of any spurious signals (hum, noise, etc.) does not exceed 50mV peak. If it does exceed this figure, it may be necessary to reduce the amplitude of the signal, so that the unwanted signal is reduced to below 50mV.

PERIOD MEASUREMENT

9. In general a period measurement is made at low frequencies only. Above 10 kc/s greater accuracy will be obtained by making a frequency measurement. (See para. 7.)

TABLE 1

POSITION OF FUNCTION SWITCH		ACCURACY	
1	PERIOD	±0.3%	± clock pulse accuracy ±1 count
10	PERIOD	±0.03%	± clock pulse accuracy ±1 count
100	PERIOD	±0.003%	± clock pulse accuracy ±1 count
1000	PERIOD	±0.0003%	± clock pulse accuracy ±1 count

(a) Table 1 details the magnitude of mean error deviations for a pure sinewave input at frequencies greater than 50 c/s. The signal amplitude should be greater than 1V r.m.s. for a.c. operation or greater than 2V r.m.s. for d.c. operation.

(b) For frequencies less than 50 c/s, the input signal level has to be increased to obtain the Table 1 accuracies. The amplitude of the r.m.s. input signal should be greater than $\frac{50}{\text{Frequency c.p.s.}}$ in volts for a.c. operation or greater than $\frac{100}{\text{Frequency c.p.s.}}$ in volts for d.c. operation.

(c) Pulse and square wave inputs should have minimum signal inputs of ±140mV peak for a.c. operation and ±2V peak for d.c. operation. They are independent of frequency over the working range of the instrument.

10. When making a period measurement, the greatest accuracy is obtained by using the fastest clock units and the maximum number of periods.

11. To make a period measurement, the following procedure should be adopted :-

(1) Set the Function switch to 1 Period.

(2) Set the Count switch to 10 mS.

(3) Set the AC-DC switch to either AC or DC depending on the signal under test. (See paras. 33 to 37.)

(4) Connect the signal to the INPUT (Red is line; Black is chassis and earth) terminals.

(5) Ensure that the frequency is lower than 30 kc/s and that the signal has sufficient amplitude (see paras. 13 to 19).

(6) Set the DISPLAY TIME control as required. If an 'infinite' display time is selected, a new counting period will not commence until the instrument is manually or externally reset. (See paras. 38 to 40.)

(7) Increase the clock unit rate by turning the Count switch in an anti-clockwise direction to 1 millisecond, 100 microseconds, 10 micro-seconds and 1 microsecond positions until the display fills all six indicators.

(8) If still greater accuracy is required, increase the number of periods measured to 10, 100 or 1000. Any overspill of digits may be checked by reducing the clock unit rate.

(9) The period of the unknown frequency is given by :-

$$\text{Period in seconds} = \frac{\text{Displayed Count X Clock Units in Seconds}}{\text{Number of Periods Measured}}$$

(10) The frequency of an unknown frequency is equal to the reciprocal of the period measurement and is given by :-

$$\text{Frequency in cycles per second} = \frac{\text{Number of Periods Measured}}{\text{Displayed Count X Clock Units in Seconds}}$$

12. Periods down to 2 microseconds may be measured in the single period position, but such measurements are usually made in the Time-Interval mode. (See paras. 20 and 21.)

WARNING : PERIOD measurements are subject to random variations if noise or hum, generated externally or internally, is present on the input signal. Thus, it is important to eliminate, if possible, external sources of such unwanted signals in order to attain accurate results. In the case of hum voltages, this can be achieved by avoiding earth loops etc., keeping all leads as short as possible and if necessary inserting an isolating transformer between the signal source and the INPUT terminals of the instrument.

NON-SINUSOIDAL INPUT SIGNALS : FREQUENCY AND PERIOD MEASUREMENT

13. It is possible to count the frequency of non-sinusoidal waveforms even though the amplitude is less than $\pm$2V. Such signals may be applied to the a.c. amplifier via a suitable differentiating network.

14. If the signal is not symmetrical, either the peak positive amplitude or the peak negative amplitude, both referred to the mean level, may be much less than half the peak-to-peak amplitude.

15. If, for example, the signal consists of short positive pulses as shown in fig. 2.2 (a), the negative excursion below the mean level is given by the peak-to-peak amplitude V multiplied by the ratio of the pulse width t_1, to the periodic time t_2 i.e. $V.t_1/t_2$; for this to be greater than 100 millivolts, the required peak-to-peak amplitude must be greater than $100.t_2/t_1$ millivolts. It should be noted that if t_2 is much greater than t_1, the required peak-to-peak amplitude is many times 100 millivolts.

16. In the case of rectangular pulse input signals, an improvement in sensitivity may be obtained by applying the input signal via an external differentiating network as shown in fig. 2.2(b).

17. If the time constant CR is chosen to be approximately half the pulse width, the negative excursion below the mean level is considerably increased as shown in fig. 2.2(c).

18. The value of the capacitor used should be not less than 1000pF, and the value of the resistor chosen accordingly. For d.c. operation the signal input should exceed 2 volts.

19. The above method makes it possible for the time-interval between two widely separated pulses, that have insufficient amplitude for d.c. operation, to be measured. This is not possible if the input signal is applied directly to the INPUT terminals.

NOTE : When pulse input signals are applied to the instrument with or without an external differentiating network, the pulse width should be greater than 1 microsecond and less than 100 milliseconds.

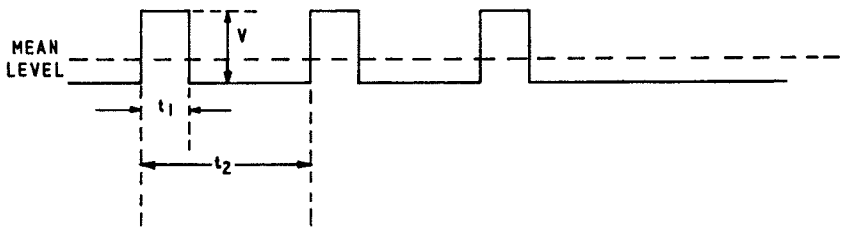
TIME-INTERVAL

Single-Line Input

20. (1) Link the START and STOP terminals and apply the signal between these linked terminals and the black input terminal.

(2) Ensure input is a positive pulse having an amplitude between 8V and 12V, with a maximum rise-time of 0.2 microseconds and minimum width of 0.5 microseconds. The time-interval must be within the range 2 microseconds to 10^4 sec.

NOTE : The maximum amplitude limitation assumes a low-impedance pulse source and refers to the voltage present at the input terminals. If



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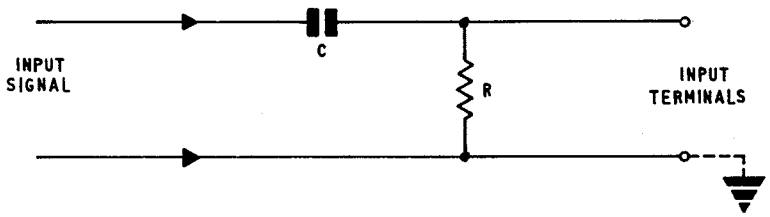

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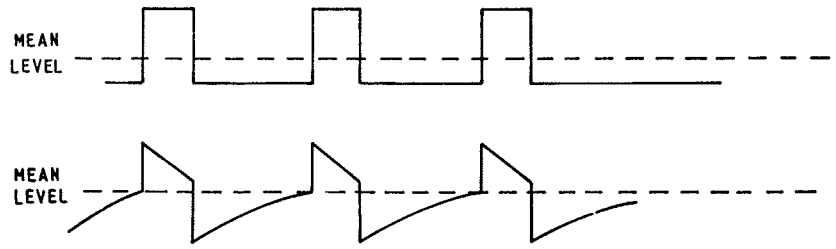

c

102/21 Input Waveforms and Circuit Fig. 2·2

the source is high, this upper limit can be raised e.g. 3kΩ source and 50V peak pulse.

(3) Set Function switch to EXTERNAL.

(4) Set Count switch to the required clock units.

(5) Set the DISPLAY TIME control to 'infinite' and press the RESET button.

(6) The time-interval T is then given by

T = DISPLAYED COUNT X CLOCK UNITS.

(7) Fresh readings may be obtained by pressing the RESET button.

Double-Line Input

21. (1) Connect the START and STOP lines to the START and STOP terminals respectively.

(2) Proceed then as for Single-Line operation, paragraphs 20 (2) to 20 (7).

TOTALIZING

External Control

22. In this mode, the number of cycles occurring externally between successive start and stop pulses may be registered. Single or double-line operation may be used.

23. (1) Apply control signals to the START and STOP lines.

(2) Set the Count switch to FREQUENCY.

(3) Set the Function switch to EXTERNAL.

(4) Apply cycles or pulses to be totalized to the INPUT terminals.

(5) Set the DISPLAY TIME control to 'infinite' and press the RESET button.

(6) The count indicated is the number of pulses that occur between successive start and stop pulses.

(7) Fresh readings may be obtained by pressing the RESET button.

Manual Control

24. In this mode, the number of cycles occurring externally between pressing the START and STOP buttons may be registered.

25. (1) Set the Count switch to FREQUENCY.

(2) Set the Function switch to EXTERNAL.

(3) Apply cycles or pulses to be totalized to the input terminals.

(4) Set the DISPLAY TIME control to 'infinite' and press the RESET button.

(5) The count indicated is then the number of pulses that occur between pressing the START and STOP buttons.

NOTE : The RESET pushbutton must be operated before making a further totalizing measurement. The instrument does not display the sum of a series of totalizing operations.

INT./EXT. STANDARD

26. During normal operation, the INT./EXT. STANDARD switch, at the rear of the unit, should be set to the INT. position.

27. If an external standard is required proceed as below :-

(1) Set INT./EXT. STANDARD switch to EXT.

(2) Connect external standard to appropriate socket at the rear of the instrument.

(3) Check that the amplitude of the external frequency is at least 1.0V r.m.s. and less than 20V r.m.s. (If the amplitude exceeds 10V r.m.s. the source impedance should be greater than 2 kilohms.)

NOTE : The external standard must have a frequency of 1 Mc/s $\pm$1%.

EXTERNAL OUTPUTS

Standard Frequencies

28. Frequencies of 1 Mc/s, 100 kc/s, 10 kc/s, 100 c/s are obtainable at the rear of the instrument from the socket market CLOCK OUTPUT. These frequencies may be selected by setting the Count switch to the appropriate position.

POSITION OF COUNT SWITCH	CLOCK OUTPUT	PULSE WIDTH
1μS	1 Mc/s	0.5μS
10μS	100 kc/s	5μS
100μS	10 kc/s	6μS
1 mS	1 kc/s	6μS
10 mS	100 c/s	6μS

29. The clock output is a negative pulse of about 12V amplitude; the width depends upon frequency as detailed in the above table.

Printer Control Signals

30. The SA.7535 may be used in conjunction with a serializer (Racal Type SA.538B) to drive a printer. For this purpose the SA.538B is connected to the printed wiring plugs on the XK/A, XF, XG, and XE/A boards; these plugs are located at the back of the SA.7535 behind the instruction panel.

31. The terminals on the XK/A printed wiring board provide the following facilities :

(a) Pin 1, Reset Inhibit. If held at zero volts by a contact or an 'on' transistor. No manual reset is possible.

(b) Pin 2, Manual Reset. Connected to EXT. RESET socket (para. 41).

(c) Pin 3, the C.F.F. Output. This is a positive pulse of 0.1 sec., 1 sec. or 10 sec., as selected by the Function switch.

(d) Pin 4, Display Hold. If held at between +1V and +12V, the display stays on and no resetting action takes place.

(e) Pin 5, Bulb Hold. If connected to -12V via a 100-ohm resistor, the display stays on whilst counting and normal resetting takes place. It is particularly useful for time-interval measurements.

(f) Pin 6 provides -12V at 20mA as an auxiliary supply.

(g) Pin 7 provides +12V at 10mA as an auxiliary supply.

(h) Pin 8 provides -15V at 20mA as an auxiliary supply.

NOTE : The total current must not exceed 30mA for auxiliary supplies.

(j) Pin 9 is zero volts (earth).

(k) Pin 10, Automatic Reset Pulse. This pin is normally at +11V and falls to -11V for about 300 microseconds when resetting takes place. Current of up to 5mA may be taken from this pin.

32. The printed wiring plug pins on the XF, XG, and XE/A boards are in parallel with the display bulbs and will provide read-out levels for the serializer.

AMPLIFIER SELECTION

33. The AC/DC switch on the front panel selects either the a.c. or d.c. amplifier. The choice of amplifier depends upon the amplitude, waveform and frequency of the signal to be measured.

34. The a.c. amplifier is selected when :-

(a) The signal frequency lies between 10 c/s and 3 Mc/s. (Para. 9.)

(b) The input amplitude is within the range of 140mV to 250V r.m.s. (reducing below 50 c/s to 100V r.m.s. at 10 c/s).

(c) The waveform has a mark-space ratio of about 1:1 (see paras. 13 to 19).

35. When switched to the a.c. amplifier the signal waveform may be superimposed on a direct voltage providing the peak amplitude does not exceed 400V.

36. The d.c. amplifier is selected when :-

(a) The signal frequency lies between 0 and 3 Mc/s.

(b) The input amplitude is within the range of $\pm$2V peak-to-peak to $\pm$200V peak-to-peak.

(c) The waveform may be any shape.

37. When switched to the d.c. amplifier, level shifting may be required to ensure that the voltage level swings at least 2V either side of earth.

DISPLAY TIME

38. The display time may be varied from 0.5 to 10 sec. approximately or made infinite by the adjustment of the control at the top right-hand side of the instrument.

39. When the control is fully counter-clockwise with the switch turned to the 'infinity' position, the display will remain unchanged unless reset either by a suitable external pulse or by pressing RESET button.

40. When fully counter-clockwise, the display time is about 10 sec. and when fully clockwise the display time is about 0.5 sec.

RESET

41. The display and count may be reset by pressing the RESET button or by applying a suitable positive pulse of 6V to 15V amplitude with 1 microsecond width and 5 microseconds maximum rise-time to the EXT. RESET socket at the rear of the unit. (See Waveforms (a) and (b) fig. 27.)

CHAPTER 3

PRINCIPLE OF OPERATION

CONTENTS

CHAPTER 3

PRINCIPLE OF OPERATION

INTRODUCTION

1. The purpose of this description is to show briefly the principles on which the instrument functions. The system can be divided into three main sections (fig. 1) viz. timebase chain, control and the totalizer chain; the totalizer chain includes the decade and display systems.

TIMEBASE CHAIN

2. Figure 1 shows a simplified block diagram of the instrument. The timebase chain consists of a 1 Mc/s crystal-controlled oscillator whose output is fed to a chain of seven divide-by-ten circuits via a shaper stage. The purpose of the timebase chain is to produce accurately timed gating pulses for making frequency measurement and clock pulses for making period measurements.

3. The output from the first four divide-by-ten circuits is applied to the last three divide-by-ten circuits via switch SB1B and an 'or' gate in the control system. The switch wafer SB2B enables one, two or all three of the last three divide-by-ten circuits to be utilized for frequency and period measurements; in the PERIOD position, a gating pulse is produced at switch wafer SB2F for each cycle of the input signal or for each 10, 100 or 1000 cycles by employing either one, two or all three of the last three dividers in the chain.

CONTROL SYSTEM

4. The control system has the following functions :

   (a) To produce a pulse for opening and closing the signal gate to the totalizer chain.

   (b) To produce a pulse for inhibiting the display during the counting and resetting operations.

(c) To produce a pulse for inhibiting the last three divide-by-ten stages, in the timebase chain, during the display and resetting operations.

(d) To produce a pulse for resetting the instrument for a new counting operation.

TOTALIZER, DECODER AND DISPLAY

5. The input signal is applied via an amplifier and a shaper to the totalizer chain for frequency measurement or, either directly or via part of the timebase chain, to the control system for period measurement; the above requirements are carried out by the Function switch SB.

6. The totalizer chain consists of six units connected in cascade which combine the functions of decade division, decoding and display.

FREQUENCY MEASUREMENT

7. The signal whose frequency is to be measured is applied to the signal input socket and fed via switch SA1B to the amplifier and shaper and then via switch SA2B and a further shaper to the signal gate in the control system. Following a reset action, the timebase starts counting pulses derived from the 1 Mc/s oscillator; at the same instant, the signal gate is opened and hence the signal has access to the totalizer chain. After a preset time of 0.1, 1 or 10 seconds (counting period), the control system emits an end-of-count output which closes the signal gate. Hence for a known period of time, cycles of the unknown frequency have been counted by the totalizer chain and hence the displayed count is a measure of the frequency. After a display period, a further resetting action occurs to initiate a new counting process.

PERIOD MEASUREMENT

8. The frequency under measurement is applied to the INPUT terminals on the front of the instrument and passed via switch SA1B, the amplifier and shaper, and switch SB1B to the control system where it opens and closes the signal gate. On opening the signal gate, clock pulses derived from the timebase chain are allowed to pass to the totalizer chain and are counted and displayed; thus, the displayed count is a measure of the time between one, ten, one-hundred or one-thousand cycles of the applied signal as determined by the setting of switch SB.

INSTRUMENT TEST

9. The operation of the instrument when performing the instrument test is the same as for frequency measurement except that the signal input is derived from the

1 Mc/s crystal oscillator via switch SA1B. Hence the instrument counts internally generated clock pulses and the displayed count provides an indication of correct operation. Since the clock pulses pass through the amplifier and shaper the entire instrument is checked.

EXTERNAL START/STOP

10. When the instrument is used with externally applied start and stop pulses, either manually or electronically derived, the input signals are passed to the totalizer chain via the signal gate in the control system. The external gating pulses (start and stop) operate in the same manner as the pulses derived from the timebase chain when the instrument is used in the frequency mode. Thus cycles of the unknown frequency are counted for a known time-interval and displayed by the totalizer chain; conversely, clock pulses from the timebase may be applied to the totalizer and an indication of the gating period is then provided.

CHAPTER 4

CIRCUIT DESCRIPTION

CONTENTS

CHAPTER 4

CIRCUIT DESCRIPTION

INTRODUCTION

1. The following circuit descriptions are confined to the manner in which the separate units function; no reference is made to the application of the units when related to the overall operation of the instrument (Overall Description, paras. 83 to 111).

2. A large proportion of the circuitry used in this instrument is in the form of bi-stable and mono-stable flip-flops employing transistors as two-state devices i.e. the transistor is either conducting or non-conducting. In order to simplify the style of circuit description, the conducting state will be referred to as 'on' and the non-conducting state as 'off'.

PRINTED WIRING BOARDS

Oscillator and Divider Type XJ (Figs. 2 and 4)

3. This unit consists of a crystal-controlled oscillator operating at a frequency of 1 Mc/s followed by a shaper and two divider stages giving an output frequency of 100 kc/s.

4. VT1, VT2 and associated circuitry form a conventional Butler oscillator. VT1 is a grounded-base stage whose operating current is stabilized by the current through the emitter resistor R1. The signal amplitude at the collector of VT1 is limited to a peak-to-peak value of approximately 1 volt by the conduction of the back-to-back diodes MR1 and MR2 which are coupled to the collector of VT1 by capacitor C1; this signal is directly coupled to the base of VT2.

5. For the purposes of this description, VT2 may be considered as a grounded-collector stage i.e. R5 may be assumed to be of zero resistance. The operating point of VT2 is stabilized by the current through R3 and R4, the junction of these resistors being decoupled by capacitor C2. Signals of comparable amplitude to those at the collector of VT1 are produced at the emitter of VT2, the oscillatory loop being completed by the feed-back through the series resonant crystal XL1 and the variable capacitor CV1, both of which are situated on the power control unit. The drive level

to the crystal is thus kept low due to the clamping effect of the diodes MR1 and MR2. The variable capacitor enables the oscillator frequency to be adjusted to exactly 1 Mc/s. Resistor R5 is included so that an output may be taken at a point which is insensitive to loading.

6. The shaper stage consists of an emitter-follower (VT3) and a grounded-emitter (VT4) with their associated components. The base of VT3 is normally held at approximately -6V by the potential divider R6, R7. Positive-going pulses on the base of VT3 appear at the emitter and cause VT4 to be cut off; negative-going pulses at the same point saturate VT4.

7. The divide-by-ten circuitry of this unit comprises two separate dividers, VT5, VT6, forming a conventional binary circuit; VT7, VT8 and VT9 make up a synchronous divider circuit.

8. Transistors VT5 and VT6 are cross-coupled by the R-C networks C6, R14 and C7, R15 to form a conventional flip-flop. The stage can therefore be stable in either of two states namely, VT5 'on' (its collector near zero potential) and VT6 'off' (its collector at approximately -10 volts) or vice versa. Steering networks are provided on each transistor.

9. Consider the binary to be in the state of VT5 'on' and VT6 'off'; the collector of VT5 will be at approximately zero potential, and the collector of VT6 at about -10 volts. If a positive pulse of about 10 volts amplitude is applied to the junction of C5 and C8, the potential at the base of VT5 will rise to about +0.2 volts, causing it to be turned 'off'. As VT5 goes 'off', its collector goes to -10 volts, biasing the base of VT6 negatively and causing VT6 to go 'on'. A second succeeding positive pulse at the junction of C5, C8 will have no effect on VT5, but will cause transistor VT6 to be turned to its 'off' state hence returning the binary to its original state. A negative pulse is passed to the base of transistor VT7 every time VT6 is 'cut off'. Diodes MR4 and MR6 are included to limit the voltage swing on the bases of VT5 and VT6, thus increasing the speed at which the binary will operate.

10. The second divider circuit, VT7, VT8 and VT9 forms a synchronous divider designed to run at a fixed input frequency of 500 kc/s which is derived from the output of the preceding binary divider VT5 and VT6.

11. Consider the circuit to be in its stable state with VT7 'off' and VT8 'on'. A negative pulse on the base of VT7 will cause this transistor to start conducting; the resultant positive pulse passed to the base of VT9 causes this transistor to be turned 'off'. VT7 is held 'on' by the current through MR11 and R24 and C9 starts to discharge through R25 and RV1. Whilst the circuit is in its mono-stable state, successive negative pulses will have no effect on VT7 as its base is already at a negative potential. A regenerative action occurs 9.5 microseconds after the circuit is triggered, and the circuit is returned to its stable state of VT7 'off' and VT9 'on'.

12. When transistor VT7 is turned 'off', the emitter-follower VT8 conducts ensuring a rapid re-charging of C9; at all other times VT8 is non-conducting due to the small current flow through MR10. The diode MR12 prevents the base of VT9 from being taken so far positive as to cause damage. The circuit is now in a condition to be triggered again by the next negative pulse emanating from VT6; since the monostable period of the circuit is 9.5 microseconds this will be the fifth after the initial pulse which triggered VT7. Hence a negative pulse at a frequency of 100 kc/s is available at the emitter of VT8 and at Tag J.

Decade Divider Type XD (Figs. 5 and 7)

13. This unit comprises a scale-of-ten frequency divider producing one output pulse for every ten input pulses. The input pulse may be at any frequency up to a maximum of 50 kc/s and provision is made for resetting the unit to the 'decimal nine' state.

14. The basic element in the unit is a binary or scale-of-two circuit. VT1 and VT2, in figure 7, and the components associated with it, form one such circuit, designated A. Transistors VT1 and VT2 are cross-coupled by the R-C networks R6, C3 and R3, C2 to form a conventional flip-flop. The flip-flop can thus be stable in either of two states namely, VT1 'on' (its collector at or near zero potential) and VT2 'off' (its collector at approximately -10 volts), or vice versa. Steering networks (MR1, R1, C1, etc.) are provided on each transistor.

15. Consider that the binary is in the state of VT1 'on' and VT2 'off'; the collector of VT1 and hence the junction of R1, C1 is at approximately zero potential and the collector of VT2 and hence the junction of R8, C4 is at approximately -10 volts. If a positive pulse or edge of amplitude say 10 volts, is applied at the input (tag C), the junction of R8, C4 will only rise to about zero potential, hence MR2 will not conduct and this input will have no effect on VT2. However, the junction of R1, C1 will rise to approximately +10 volts; MR1 will then conduct, and VT1 will be turned 'off' which in turn switches VT2 'on'. Hence, the binary will change to a state with VT1 'off' and VT2 'on'. After the time-constants C1, R1 and C4, R8 have settled to their new potentials, a second input pulse will switch the binary back to the original state in a similar manner.

16. The output from binary A (VT2 collector) is fed to the input of binary B and similar couplings are made from binaries B to C and C to D to form a chain of four binaries connected in cascade. Such a chain would form a scale-of-sixteen divider; that is, for every sixteen pulses applied to the input, one pulse would appear at the output. However, feedback from binary D to binaries B and C convert it to a scale-of-ten.

17. In the initial condition of the circuit, representing a count of 'decimal nine', all four binaries are in the state in which the left-hand transistors (VT1, VT3, VT5 and VT7) are 'on' and the right-hand transistors (VT2, VT4, VT6 and VT8) are 'off'. After a count, the circuit can be reset to this state independently of signals on

the input (tag C) by taking tag A momentarily from its normal potential of +12 volts to approximately -12 volts. Current will then flow through R2, R10, R18 and R27 in such a direction as to turn 'on' VT1, VT3 etc.

18. The first input pulse applied to tag C switches VT1 'off' and VT2 'on' causing the collector of VT2 to rise from approximately -10 volts to zero potential; this positive edge is applied to the input of binary B, switching VT3 'off' and VT4 'on' to develop a positive edge at the output (tag D). The unit is now in the state of 'decimal 0' as shown in figure 5.

19. Successive input pulses switch binary A from one state to the other, whilst binary B changes state each time VT2 is switched 'on' (i.e. every two input pulses); binary D is thus triggered when VT6 is switched 'on' i.e. at 'decimal eight'. As VT6 goes 'on' it switches VT7 'on', and the positive edge at the collector is differentiated by C13 and R25 and applied through diodes MR5 and MR8 to the bases of VT4 and VT6 which are thus turned 'off'. A further input pulse switches binary A in order to revert the unit to the 'decimal nine' state; it has thus completed a cycle in ten input pulses. Note that no effect is produced by the feedback network when VT7 is switched 'off' since the negative edge so produced at the junction of C13, R25 drives the diodes MR5 and MR8 into the cut-off condition hence producing no effect on transistors VT4 and VT6.

TABLE 1

Binary States - XD Unit

Decimal	9	0	1	2	3	4	5	6	7	8	9
VT1	+	-	+	-	+	-	+	-	+	-	+
VT2	-	+	-	+	-	+	-	+	-	+	-
VT3	+	-	-	+	+	-	-	+	+	+	+
VT4	-	+	+	-	-	+	+	-	-	-	-
VT5	+	-	-	-	-	+	+	+	+	+	+
VT6	-	+	+	+	+	-	-	-	-	-	-
VT7	+	-	-	-	-	-	-	-	-	+	+
VT8	-	+	+	+	+	+	+	+	+	-	-

20. Table 1 shows the state of all the transistors in the circuit after each pulse; a plus sign indicates that the transistor in question is 'on' and its collector is at approximately zero potential; a minus sign indicates that the collector is at approximately -10 volts.

21. If the output at tag D is coupled to the input of a similar succeeding XD unit it will send to such a unit a carry pulse every time the unit changes from the 'decimal nine' to zero state.

Synchronous Divider Type XH (Figs. 8 and 10)

22. This unit consists of three cascaded decade divider circuits giving a final output frequency of 100 c/s from an input frequency of 100 kc/s. The dividers are of the synchronous type i.e. they are designed to run at a fixed frequency only.

23. The first frequency divider circuit VT1, VT2 and VT3 develops an output frequency of 10 kc/s, at pin J, derived from the input frequency of 100 kc/s at pin F. This circuit is basically a mono-stable multi-vibrator whose mono-stable time is accurately set to 95 microseconds. Consider the circuit to be in its stable time i.e. with VT1 'off' and VT3 'on'. The collector of VT1 and the emitter of VT2 will then be at approximately -12 volts. The next negative-going pulse on the base of VT1 causes it to conduct and a regenerative action is initiated whereby a positive edge is passed via C2 to the base of VT3 thus turning VT3 'off'. VT1 is then held 'on' by the current passing through R6 and R7, and C2 starts to discharge through R8 and VR1. Meanwhile, a succeeding positive edge appearing across R1 cannot be passed to VT1 since MR1 is then cut-off; similarly, negative edges, although passed to the base of VT1, have no effect since VT1 is now 'on'. 95 microseconds after the circuit is triggered by the first negative pulse, C2 is discharged to the point where VT3 starts to conduct; a regenerative action is initiated and the circuit returns to its stable state with VT1 'off' and VT3 'on'. When VT1 turns 'off', the emitter-follower VT2 conducts ensuring a rapid recharge of C2; at all other times VT2 is turned 'off' since the current through R4 is then very small. The circuit is now ready to be triggered again by the next negative pulse on the input (pin F), and since the mono-stable period is 95 microseconds, this will be the tenth pulse after the initial pulse which triggered VT1. Hence, a negative pulse approximately 5 microseconds wide at a frequency of 10 kc/s is available at the emitter of VT2 and at pin J.

24. The following divider, comprising VT4, VT5 and VT6, is virtually identical to the preceding one except that C4 has ten times the capacitance of C2. The mono-stable period of this divider is 950 microseconds and its output frequency is thus 1 kc/s.

25. The third circuit is again a duplicate of the first and second except for a further ten-fold increase in the value of the capacitance C6 and C7 thus giving an output frequency of 100 c/s.

26. The stability of the timing components in the dividers is such that the preset controls VR1, 2 and 3 require only initial setting-up, after manufacture, in order to take up component tolerances. Further adjustment should only be required if components have been replaced.

Totalizer, Decoder and Display Unit Type XG (Figs. 11 and 13)

27. This unit consists of two sections, the totalizer and the display or read-out stages which also have facilities for external recognition lines.

28. Totalizer : The totalizer is a scale-of-ten frequency divider which produces one output pulse for every ten input pulses. The input signal may be any frequency up to a maximum of 300 kc/s, and provision is made for resetting the chain to the 'decimal zero' state.

29. The basic element is a binary or scale-of-two circuit, VT3 and VT4, designated A. Transistors VT3 and VT4 are cross-coupled by the networks R8, C10 and R3, C9 to form a conventional flip-flop. The flip-flop can thus be stable in either of two states namely, VT3 'on' (its collector at near zero potential) and VT4 'off' (its collector at approximately -10 volts), or vice versa. Steering networks (MR1, R1, C1 etc.) are provided on each transistor.

30. Consider the binary to be in the state VT3 'on' and VT4 'off'; the collector of VT3 and hence the junction of R1, C1 is at approximately zero potential and the collector of VT4 and hence the junction of R10, C2 is at approximately -10 volts. If a positive pulse or edge, of amplitude say 10 volts, is applied to the input (tag H), the junction of R10 and C2 will only rise to about zero potential; hence MR4 will not conduct and this input pulse will have no effect on VT4. However, the junction of R1, C1 will rise to approximately +10 volts, MR1 will then conduct and VT3 will be turned 'off' and VT4 'on'. After the time-constants C1, R1 and C2, R10 have settled to their new potentials, a second input pulse will switch the binary back to the original state in a similar manner. It should be noted at this point that VT1 and VT2 have no effect on the action of binary A.

31. The output from binary A (VT4 collector) is fed to the input of binary B and similar couplings are made from binaries B to C and C to D to form a chain of four binaries connected in cascade. Such a chain would form a scale-of-sixteen divider; however, feedback from binary D to binaries B and C converts it to a scale-of-ten divider.

32. In the initial condition of the circuit, representing a state of 'decimal zero', binary A is in the state VT3 'off' and VT4 'on' and binaries B, C, and D are in the state in which the left-hand transistors (VT5, VT7, VT9) are 'on' and the right-hand transistors (VT6, VT8, VT10) are 'off'. After a count, the circuit can be reset to this state independently of signals on the input (tag H) by taking tag A momentarily from its normal potential of +12 volts to approximately -12 volts. Current will then

flow through R7, R12, R20 and R29 in such a direction as to turn 'on' VT4, VT5, VT7 and VT9.

33. The first input applied to tag H switches VT3 'on' and VT4 'off' causing the collector of VT4 to fall from approximately zero potential to -10 volts; this negative edge is applied to the input of binary B, but will have no effect on VT5 or VT6, MR5 and MR6 being biased off.

34. A second input pulse applied to tag H switches binary A back to its original state (VT3 'off', VT4 'on') and develops a positive edge at the collector of VT4; this edge, applied to the input of binary B, switches VT5 'off' and VT6 'on' to develop a positive edge at VT6 collector which is in turn applied to the input of binary C; binary C similarly changes state and triggers binary D. The chain is now in the state of 'decimal 2' as shown in figure 11.

35. Successive input pulses switch binary A from one state to the other, whilst binary B changes state each time VT4 is switched 'on' (i.e. every two input pulses), and binary C changes state each time VT6 is switched 'on' (i.e. every four input pulses). Binary D is thus triggered when VT8 is switched 'on' i.e. on the tenth input pulse and a positive edge is produced at the output (tag J). When VT9 is switched 'on' the positive edge at the collector is differentiated by C17 and R27 and applied through diodes MR7 and MR10 to the bases of VT6 and VT8 which are thus turned 'off'. It has thus completed a cycle in ten input pulses. Note that no effect is produced by the feedback networks when VT9 is switched 'off' since the negative edge so produced at the junction of C17 and R27 drives the diodes MR7 and MR10 into the cut-off condition producing no effect on transistors VT6 and VT8.

TABLE 2

Binary States - XG Unit

Decimal	0	1	2	3	4	5	6	7	8	9	0
VT3	-	+	-	+	-	+	-	+	-	+	-
VT4	+	-	+	-	+	-	+	-	+	-	+
VT5	+	+	-	-	+	+	-	-	+	+	+
VT6	-	-	+	+	-	-	+	+	-	-	-
VT7	+	+	-	-	-	-	+	+	+	+	+
VT8	-	-	+	+	+	+	-	-	-	-	-
VT9	+	+	-	-	-	-	-	-	-	-	+
VT10	-	-	+	+	+	+	+	+	+	+	-

36. Table 2 shows the state of all the transistors in the circuit after each pulse; a plus sign indicates that the transistor in question is 'on' and its collector is at approximately zero potential; a minus sign indicates that the collector is at approximately -10 volts.

37. Read-Out Circuit : The read-out circuits comprise transistors VT1 and VT2 which, operating in conjunction with the read-out gates, switch 'on' the appropriate output transistor controlling the display bulb.

38. The emitter of VT3 is directly connected to the base of VT1 and to the anode of diode MR2; this point is thus clamped at near earth potential by the forward conduction of either the base/emitter junction of VT1 or by MR2. The operation of VT3 is thus unaffected by the connection of this point to VT1 and MR2 rather than directly to earth. The emitter of VT4 is similarly connected to the base of VT2 and the anode of MR3. When VT3 is 'on', the greater part of its emitter current flows into the base of VT1 which is thus turned hard 'on'; when VT3 is 'off', the current through R5 and MR2 takes the base of VT1 slightly positive thus turning it 'off'. VT2 is switched in a similar manner by the action of VT4.

39. The collectors of VT1 and VT2 are directly connected, respectively, to the emitters of VT13, VT16, VT19, VT22, VT25, and VT11, VT14, VT17, VT20, VT23. Thus when binary A is in the state VT3 'on' and VT4 'off', VT1 is 'on' and the emitters of VT13, VT16, VT19, VT22 and VT25 are held at near earth potential.

40. Read-Out Gates : VT12, VT15, VT18, VT21 and VT24 are emitter-followers, each with a potential divider on its emitter, feeding the paralleled bases of output transistor pairs VT11, VT13 and VT14, VT16 etc.; the bases of the emitter-followers are fed via 'and' gates from the binary stages B, C and D.

41. Consider R39 and MR13 on the base of VT15. The anode of MR13 is connected to the collector of VT7, and R39 to the collector of VT5; if both connections are at zero potential, the base of VT15 will also be at zero potential. With the base of VT15 at zero volts, the junction of R40, R41 and hence the bases of VT14 and VT16 will be positive and hence VT14 and VT16 will be 'off'. If the junction of R39 and the collector of VT5 is at zero potential while the junction of MR13 anode and VT7 collector is at -10 volts, MR13 will be cut-off and the base of VT15 will remain at zero potential. If, conversely, the potential at VT5, R39 junction is -10 volts and MR13, VT7 junction is zero then MR13 will conduct and hold the base of VT15 at zero potential. If, however, both junctions are at -10 volts, the base of VT15 will be sufficiently negative to hold the junction of R40 and R41 negative; hence, either VT14 or VT16 will be 'on'. Thus R39 and MR13 form an 'and' gate to negative signals.

42. Similar gates are connected to VT18 and VT21. In the case of VT24 there are three inputs to the base via R48, MR16 and MR17; all three inputs must be negative for the base of VT24 to go negative. In the case of VT12, the drive is via R36 from the collector of VT10.

Note that no effect

TABLE 2a

Read-Out, Flip-Flop and Emitter-Folower States - XG Unit

Decimal	Read-Out		Flip-Flop						Emitter-Followers				
			B		C		D						
	VT1	VT2	VT5	VT6	VT7	VT8	VT9	VT10	VT12	VT15	VT18	VT21	VT24
0	OFF	ON	+	-	+	-	+	-	-	+	+	+	+
1	ON	OFF	+	-	+	-	+	-	-	+	+	+	+
2	OFF	ON	-	+	-	+	-	+	+	-	+	+	+
3	ON	OFF	-	+	-	+	-	+	+	-	+	+	+
4	OFF	ON	+	-	-	+	-	+	+	+	-	+	+
5	ON	OFF	+	-	-	+	-	+	+	+	-	+	+
6	OFF	ON	-	+	+	-	-	+	+	+	+	-	+
7	ON	OFF	-	+	+	-	-	+	+	+	+	-	+
8	OFF	ON	+	-	+	-	-	+	+	+	+	+	-
9	ON	OFF	+	-	+	-	+	-	+	+	+	+	-

+ infers an output voltage of approximately zero potential.

- infers an output voltage of approximately -10 volts.

43. Table 2a shows the states of the read-out transistors VT1, VT2, the flip-flops B, C, D and the emitter-followers feeding the output transistors. The emitter of VT12 is negative only during the decimal states 0 and 1; the emitter of VT15 is only negative during the decimal states 2 and 3, etc.

44. Consider that the flip-flops are in the 'decimal zero' state then VT12 emitter is negative; VT2 is 'on' and thus VT11 is 'on'; 1LP1 shows on the display scale (provided that the bulb supply at tag P is at -12 volts); VT13 will be 'off' since no emitter current is available from VT1. The remaining output transistors will be 'off' since their bases are held slightly positive by transistors VT15, VT18, VT21 and VT24 and any one can be turned 'on' by the appropriate combination of drive to its emitter from VT1 or VT2 and to its base from the appropriate emitter-follower.

45. It should be noted, when referring to the waveforms (fig. 11), that in normal operation the bulb supply is off while the unit is counting. Thus, the waveforms as shown for the collectors of VT1, VT2, VT11, VT13, VT14, etc. cannot be observed unless special provision is made for switching on the bulb supply during operation.

Totalizer, Decoder and Display Unit Type XF (Figs. 11 and 15)

46. This unit is identical in function to the XG unit but differs in certain component changes which limit the maximum operating frequency to 50 kc/s. For details of the operation of the unit, read the description of the XG unit (paras. 27 to 45).

Totalizer, Decoder and Display Unit Type XE/A (Figs. 16 and 18)

47. This unit consists of two sections, the totalizer and the display or read-out chain stages.

48. Totalizer : The totalizer is a scale-of-ten frequency divider producing an output pulse for every ten input pulses. The input signal may be of any frequency up to a maximum of 3 Mc/s and provision is made for resetting the stage to the 'decimal zero' state.

49. The basic element is the binary or scale-of-two circuit; VT1, VT4 and the components associated with them form one such circuit designated A. Transistors VT1 and VT4 are cross-coupled by the networks R10, C4 and R2, C1 to form a conventional flip-flop. The flip-flop can thus be stable in either of two states, namely with VT1 'on' (its collector at near zero potential) and VT4 'off' (its collector at approximately -10 volts) or vice versa. Differentiating and steering networks are provided on each transistor (C2, R4, MR2, R55 and C3, R9, R56, MR7).

TABLE 3

Read-Out, Flip-Flop and Emitter-Follower States -XE/A Unit

Decimal	Read-Out		Flip-Flop						Emitter-Followers				
			B		C		D						
	VT2	VT3	VT11	VT13	VT17	VT19	VT23	VT25	VT6	VT10	VT15	VT20	VT24
0	ON	OFF	-	+	-	+	-	+	-	+	+	+	+
1	OFF	ON	-	+	-	+	-	+	-	+	+	+	+
2	ON	OFF	-	+	-	+	+	-	+	-	+	+	+
3	OFF	ON	-	+	-	+	+	-	+	-	+	+	+
4	ON	OFF	+	-	-	+	+	-	+	+	-	+	+
5	OFF	ON	+	-	-	+	+	-	+	+	-	+	+
6	ON	OFF	-	+	+	-	+	-	+	+	+	-	+
7	OFF	ON	-	+	+	-	+	-	+	+	+	-	+
8	ON	OFF	+	-	+	-	+	-	+	+	+	+	-
9	OFF	ON	+	-	+	-	+	-	+	+	+	+	-

+ implies an output voltage of approximately zero potential.

- implies an output voltage of approximately -10 potential.

50. Consider the binary to be in the state VT1 'on' and VT4 'off'; the collector of VT1 and therefore the junction of C2, R4 is at approximately zero potential; the collector of VT4 and therefore the junction of C3, R9 is at approximately -10 volts. If a positive-going pulse of 10 volts is applied to tag H, the junction of C3, R9 will rise to about zero volts, MR7 cannot conduct, and the input pulse will have no effect on VT4. However, the junction of C2, R4 will rise slightly positive. MR2 will conduct and VT1 will be turned 'off' which in turn switches VT4 'on'. Therefore the binary has changed to a state of VT1 'off' and VT4 'on'. The potentials at the junction of C2, R4 and C3, R9 will now be -10 volts and zero volts respectively. The circuit time-constants are designed to recover their new voltage levels before the next input pulse arrives and reverts the binary back to its original state in a similar manner.

51. The output from binary A (VT4 collector) is fed to the base of the inverter stage VT8; the output from the collector of VT1 is fed via C16 and MR33 to the base of VT25. In this way, the normal scale-of-sixteen division is converted to a scale-of-ten.

52. In the initial condition of the circuit representing a state of 'decimal zero', binary A is in the state VT1 'on' and VT4 'off'; binaries B, C and D are in the state in which the left-hand transistors (VT11, VT17 and VT23) are 'off' and the right-hand transistors (VT13, VT19 and VT25) are 'on'. After a count, the circuit can be reset to this state independently of signals on the input (tag H) by taking tag A momentarily from its normal potential of +12 volts to approximately -12 volts. Current will then flow through R1, R26, R40 and R51 in such a direction as to turn VT1, VT13, VT19 and VT25 'on'.

53. The operation of the decade with respect to each successive input pulse is best understood if reference is made to the waveforms of the unit (fig. 16). In the 'decimal zero' state, transistor VT25 is 'on' and whilst in this condition the inhibit diode MR30 is forward biased, thus clamping the collector of VT8 at zero potential. Negative-going edges have no effect on succeeding stages; therefore, when the first input pulse (at tag H) 'turns over' binary A, succeeding binaries are unchanged. The second pulse at tag H reverts binary A to its original state and the positive-going edge from the collector of VT1 is fed forward to the steering networks associated with VT25, thereby turning 'off' VT25. MR30 now ceases to conduct and the forward bias is removed allowing VT8 to invert the waveform appearing on its base. VT8 produces positive-going edges at the 4th, 6th and 8th input pulse thereby changing the state of binary B in each case. Positive edges change the state of binary C at the 6th and 10th input pulse, and the positive-going edges will coincide with the tenth pulse to change the state of binary D. Therefore every tenth input pulse at tag H produces a positive-going pulse at the collector of VT25, which may be fed to a succeeding totalizer.

54. Read-Out Circuits : The read-out circuits comprise transistors VT2 and VT3 which, operating in conjunction with the read-out gates, switch 'on' the appropriate transistor controlling the display bulb.

55. The emitter of VT1 is directly connected to the base of VT2 and the anode of MR3; this point is thus clamped at near earth potential either by the base-emitter junction of VT2 or by MR3. The operation of VT1 is thus unaltered by this point being connected to VT2 and MR3 rather than directly to earth. The emitter of VT4 is similarly connected to the base of VT3 and the anode of MR5.

56. When VT1 is 'on', most of its emitter current flows into the base of VT2 which is thus turned hard 'on'; when VT1 is 'off', the current through R5 and MR3 takes the base of VT2 slightly positive turning it 'off'. VT3 is switched in a similar manner by the action of VT4.

57. The collectors of VT2 and VT3 are directly coupled, respectively, to the emitters of VT5, VT9, VT14, VT18, VT22 and VT7, VT12, VT16, VT21, VT26. Thus, when binary A is in the state where VT1 is 'on' and VT4 'off', then VT2 is 'on' and the emitters of VT5, VT9, VT14, VT18 and VT22 are held at near earth potential.

58. Read-Out Gates : VT6, VT10, VT15, VT20 and VT24 are emitter-followers, each with a potential divider on its emitter, feeding paralleled bases of output transistor pairs VT5, VT7 and VT9, VT12 etc.; the bases of the emitter-followers are fed via 'and' gates from the binary stages.

59. Consider MR29 and R47 on the base of VT24. The anode of MR29 is connected to the collector of VT19, and R47 to the collector of VT13. If both junctions are at zero potential then the base of VT24 will also be at zero potential. With the base of VT24 at zero volts the junction of R48 and R49 will be positive and hence VT22 and VT26 will be 'off'. If the junction of R47 and the collector of VT13 is at zero volts and the junction of MR29 and VT19 is at -10 volts, MR29 will be cut-off and the base of VT24 will be at zero volts. However, if both junctions are at -10 volts, the base of VT24 will be sufficiently negative to hold the junction of R48 and R49 negative. Hence either VT22 or VT26 will be 'on'. Thus R47 and MR29 form an 'and' gate for negative-going signals.

60. Similar gates are connected to VT20 and VT15. In the case of VT10, there are three inputs to its base via MR10, MR11 and R15, all three of which must be negative for the base of VT10 to go negative. In the case of VT6, drive is via R7 from the collector of VT23.

61. Table 3 shows the states of the read-out transistors VT2, VT3, the flip-flops B, C, D and the emitter-follower feeding the output transistors. The emitter of VT6 is negative only during the decimal states 0 and 1; VT10 is negative only during the decimal states 2 and 3 etc.

62. Consider that the flip-flops are in the 'decimal zero' state, then VT6 emitter is negative; VT2 is 'on' and thus VT5 is 'on' and 1LP1 shows on the display scale. None of the other output transistors will be 'on' since their bases are held slightly positive by transistors VT10, VT15, VT20 and VT24. Any one of the other output

transistors may be turned 'on' by the appropriate combination of drive to its emitter from VT2 or VT3, and to its base from one of the emitter-followers.

63. It should be noted when referring to the waveforms (fig. 16) that in normal operation the bulb supply is not 'off' while the unit is counting. Thus the waveform shown for the collectors of VT2, VT3, VT5, VT7 etc., cannot be observed unless special provision is made for switching on the bulb supply during counting.

3 Mc/s AC/DC Amplifier Type XB (Figs. 19 and 21)

64. This unit comprises a two stage a.c. amplifier, a 'gating' circuit and d.c. amplifier which feeds a Schmitt trigger circuit to provide signals to the output buffer stage. The unit produces positive pulses corresponding to the applied input frequency at a fixed rise-time and 12 volts amplitude.

65. When the AC/DC switch (SE, fig. 28) is in the AC position, the input signals are fed via this switch to C2 and R2 of the power control board (fig. 31) onto the base of VT1, in the XB unit. VT1 is a common-emitter stage providing a signal at its collector which is directly connected to the base of VT2. The gain and operating points of VT1 and VT2 are stabilized by negative feed-back through R2 in the emitter circuit of VT1 and through R4 onto the base of VT1 from the junction of R5 and R6 in the emitter circuit of VT2. The effective a.c. load is R7, C2 providing bypassing down to low frequencies.

66. The output at the collector of VT2 is fed via the forward biased diode MR6 and C7 to the base of VT3. When switched to AC, no connection is made to the gating point (tag J) and hence MR6 is forward biased by the current through R22, R23 and R21.

67. When the AC/DC switch (SE) is in the DC position, the input signals are fed into the base of VT3 via a series resistor (R1, fig. 28) to tag G. The gating point (tag J) is taken to -12V resulting in the diode MR6 being reverse biased; hence the input signal is not shunted by the low value collector load of VT2. The amplitude of the positive signals on the base of VT3 is limited by MR1 to about +1V to prevent a base-emitter breakdown in VT4.

68. Transistors VT4, VT5 and associated circuitry form a conventional Schmitt trigger circuit but with the addition of clamping diodes MR2 and MR3. A potential divider between the negative 12 volt and 0 volt lines, consisting of R17, R16, R25, MR4 and the wiper of RV1, feeds the diodes to limit the voltage swing at the base of VT5 to a value determined by the forward conduction potentials of MR2, MR3 and the voltage across R16. RV1 is adjusted for fine control of the triggering points. Hence, a square wave is produced to the collector of VT5 that will correspond in frequency to that at the input. MR4 is a temperature compensating diode.

69. Transistor VT6 is the output buffer stage and operates as a grounded-emitter. In the absence of signals from VT5, VT6 is held 'off' by the current through R19, the base potential being held a fraction of a volt positive by the forward voltage drop of MR5. A positive edge at the collector of VT5 causes current flow through C5 which drives MR5 further into conduction to have no effect on VT6. A negative edge at VT5 collector is differentiated by C5 and the base-emitter junction of VT6. Thus VT6 is bottomed until the base current is reduced to about zero by the current through R19; this turns VT6 'off' and results in a positive pulse of 12 volts amplitude being produced at tag C for each negative-going edge at the collector of VT5.

Control Circuit Board Type XK/A (Figs. 22 and 24)

70. The XK/A board contains the following circuits : 'or' gate, control flip-flop, signal gate, bulb inhibit, display-time generator, reset-delay generator and reset generator. Before describing the operation of each circuit, a brief description will be given of the operation sequence. 'Start' and 'stop' pulses are applied at the 'or' gate input which trigger the control flip-flop; the flip-flop is triggered by the 'start' pulse which opens the signal gate and supplies a control potential for turning the display lamp off. When the flip-flop is reset by the 'stop' pulse, it closes the signal gate, changes the control potential for turning the display lamps on again and triggers the display-time generator. The display-time generator is a mono-stable multivibrator whose quasi-stable period is determined by a potentiometer fitted externally. Whilst the display-time generator is in its quasi-stable state, the 'or' gate is inhibited and no further control pulse may be applied to the control flip-flop. As the display-time generator resets, it triggers a reset-delay generator which holds the inhibit level on the 'or' gate for a further 18 milliseconds, and simultaneously triggers the reset generator. When triggered, the reset-delay generator allows all totalizer boards to be reset and settle down before commencing a new count.

71. 'Or' Gate : This consists of VT13 and associated components. Suppose a 'start' pulse of 10V amplitude is applied to the 'or' gate input (pin K); the negative-going edge will pass through C12 and MR18, clamping the base of VT13 at -12V; the positive-going edge will be differentiated by C12 and R38, and the emitter of VT13 which was at about -10V, will be taken to about -2V. Thus an 8V pulse will appear at the 'or' gate output (pin H).

72. Control Flip-Flop : This circuit consists of VT2, VT4 and associated components. Immediately after a reset pulse, VT2 will be 'on' and VT4 'off' and the collector potential of VT4 will be clamped at -12V by MR5. A positive-going 'start' pulse at pin C will cause the flip-flop to be triggered over, and a 'stop' pulse at pin D will reset it. The circuit is similar to the high speed binaries used in the XE/A board.

73. Signal Gate : This circuit consists of VT1, VT3 and associated components. VT1 can be regarded as an amplifier whose emitter is grounded by VT3 functioning as a switch. The base of VT1 is biased to beyond cut-off by R3 and R4. The input signal is applied via terminal F and C1 to the base of VT1. When the control flip-flop is in the "reset" or "gate closed" state, VT2 is conducting with the result that VT3 and, in turn, VT1 is prevented from conducting. When a 'start' pulse is applied to the control flip-flop, VT2 is cut off and VT3 conducts. On negative peaks of the applied signal, VT1 conducts, the collector potential rises from -12 volts to 0 volts, approximately, to produce a 12-volt positive-going pulse at pin G.

74. Bulb Inhibit : When the control flip-flop is reset, the collector of VT4 is at -12V and hence, since VT5 and VT14 are emitter-followers, the potential at pin N is about -12V and this voltage level may be used to turn display bulbs on. When the control flip-flop is triggered over, the voltage level at pin N will rise to about 0V and this may be used to turn the display bulbs off.

75. Display-Time Generator : This is a mono-stable multivibrator and consists of VT6, VT7, VT8 and the associated components. The display time is determined by C6, R22 and an external potentiometer connected between pin P and the -12V supply line. The display-time generator is triggered by a negative edge that occurs as the control flip-flop is reset. When triggered, VT6 goes 'on' and the diode MR12 clamps the emitter of VT13 at about 0V, thus inhibiting the 'or' gate.

76. Reset-Delay Generator : When the display-time generator resets, VT8 goes 'on' and triggers the reset-delay generator VT9 and VT10. The inhibit is held on the 'or' gate by MR16. The display-time generator resets after 18 milliseconds because of the time-constant of C9, R29 and R26.

77. Reset Generator : The reset generator comprises VT11 and VT12. VT11 is normally 'on' and hence the voltage at the emitter of VT12 is at about +11V. As the reset-delay generator is triggered, VT10 goes 'on' and sends a 12V pulse to the base of VT11 'off'. VT11 remains 'off' for about 350 microseconds while C11 recovers. When VT11 is 'off', its collector falls to -12V and hence the emitter of VT12 is taken to -12V. The reset pulse is thus 350 microseconds wide and approximately 21V in amplitude.

78. External Reset : If an external positive pulse of amplitude greater than 6V is applied to pin R, it is coupled via C8 and MR14 to the base of VT9 and thus initiates a reset pulse. Diode MR15 resets the display-time generator.

Power Supply (Figs. 29 and 31)

79. The mains input is applied via fuses FS1, FS2, Count switch (SA3) and the voltage selector panel to the primary winding of transformer T1 which is tapped to

accept a.c. voltages of 115, 200, 220 and 240 volts. The secondary is centre-tapped with 15 volts r.m.s. across each half. The full-wave rectifiers MR1 and MR4 supply the positive 12 volts d.c. Smoothing is effected by C4 and stabilization by resistor R10 and Zener diode MR5. Likewise the negative 12-volt supply is obtained from the full-wave rectifier circuit MR2 and MR3, smoothed by C8 and stabilized by transistor VT2 (adjacent to the voltage selector). Resistor R9, capacitor C5 and Zener diode MR6 provide the control voltage to the base of this transistor. The negative 15 volt d.c. supply is not stabilized and is taken from the reservoir capacitor C8.

80. When working from an external battery, the -15V line is strapped to the -12V line and the crystal oven may be powered from either the +12V or -12V battery by making a suitable external connection. No on-off switch is provided and the battery must be disconnected.

81. Transistor VT1 is the control transistor for the read-out bulb supply. A negative pulse from the control chain (bulb inhibit) causes VT1 to conduct, thus allowing current to be fed to the bulb.

82. Transistors VT1 and VT2 on the power control board function as an ancillary shaper between decade divider circuits and the control flip-flop on the (XK/A) board; VT3 performs a similar function on the signal gate circuit.

OVERALL DESCRIPTION (Figs. 25, 26, 27 and 28)

Introduction

83. For the purpose of the following descriptions, it is assumed that the mode of operation for each type of unit (paras. 1 to 78) is understood.

84. With reference to figure 28, the operation of the overall system can be broken down into the following parts :-

(a) Timebase Chain comprising one XJ, one XH, and three XD units.

(b) Control system comprising one XK/A unit.

(c) Totalizer, Decoder and Display comprising one XB, one XE/A, one XG and four XF units.

Timebase Chain

85. The 1 Mc/s output from the crystal oscillator is fed to four synchronous decade dividers connected in cascade; for test purposes, the 1 microsecond output from the XJ unit is fed via Count switch wafer (SA1B) and the AC/DC switch (SE) to the amplifier and shaper circuits (XB unit).

86. The 100 c/s output from the XH unit is applied, for frequency measurement purposes, via the Function switch wafer SB1B and the 'or' gate (XK/A unit) to the three scale-of-ten dividers (XD units) connected in cascade.

87. The gating pulses are derived from the 'or' gate (XK/A unit) and the three XD unit outputs, and are fed into the control system (XK/A unit) via the FREQUENCY positions of the Function switch wafer SB2B.

Control System

88. The XK/A unit control system comprises the control flip-flop, the buffer, the display-time generator, the reset-delay generator, the reset generator, the 'or' gate and the signal gate. The manner in which the sections of the control system function is most conveniently described in paragraphs 90 to 97.

Totalizer, Decoder and Display

89. The signal input circuitry includes the amplifier and shaper (XB unit) and a signal gate (XK/A unit). The input signal for either frequency or period measurement is fed from the input terminals via Count switch wafer SA1B to the AC/DC switch SE. If an a.c. signal is being measured, switch SE applies the signal to the a.c. amplifier in the XB unit and then to the d.c. amplifier and shaper in this unit. In the case of a d.c. signal measurement, switch SE applies the signal directly to the d.c. amplifier and shaper in the XB unit. The output from the XB unit is taken to the Count switch wafer SA2B, to the signal gate (XK/A unit) via a shaper circuit in the Power Control Board (when making frequency measurements) and via the Function switch wafer SB1B (when making period measurements) to the 'or' gate in the XK/A unit. When the signal gate is open, the signal is passed to the totalizer, decoder and display chain comprising one XE/A, one XG and four XF units connected in cascade. When the signal gate is next closed, the count made by the totalizer chain is displayed.

Frequency Measurement (Fig. 25)

90. This description is concerned, in the main, with the operation of the XK/A control system. Figure 25 shows the waveforms at various points in the instrument and the events which occur when making a frequency measurement.

91. With the Function switch SA in the FREQUENCY X10 position and the Count switch SB in FREQUENCY position, assume that a reset pulse (waveform K) has occurred at instant A. Waveform(a) shows a train of 10 millisecond clock pulses at the output, tag D, of the XH unit. The XD divider units are reset to 'decimal nine' and the 'or' gate is inhibited by the delay generator pulse (waveform j).

92. Following this reset pulse, at instant B, the inhibit level to the 'or' gate is removed to allow the 10 millisecond clock pulses (waveform b) through to the XD divider units. The first clock pulse at instant C sets the XD unit to 'decimal zero' and the output pulse at tag D sets the control flip-flop to the state where the positive-going output 'opens' the signal gate (waveform d). The input signal under measurement (waveform e), after shaping (waveform f), has access to the totalizer chain at tag H of the XE/A unit. The positive-going output from the control flip-flop at instant C also inhibits the display bulbs.

93. When the XD unit reaches a count of 'decimal eight', a negative-going level (waveform c) is applied to the control flip-flop which has no effect.

94. At instant D, the XD unit is in the state of 'decimal zero' and the positive-going output level at tag D (waveform c) sets the control flip-flop to the state where its negative-going output is applied to the signal gate, to the bulb inhibit and to the display-time generator to have the following effects :-

(a) Signal gate 'closes' (waveform d) so that the signal under measurement is prevented from reaching the totalizer.

(b) Removes the bulb inhibit level, to permit the power amplifier to apply the negative supply to the display bulbs.

(c) The display-time generator is set to its quasi-stable state, to provide a positive-going output pulse that inhibits the 'or' gate.

95. Toward the end of the display period, the display-time generator relaxes into its stable state (waveform h : instant A) and the positive-going output at this instant is applied to the reset-delay generator to produce a positive-going output pulse (waveform not shown but is inverse of waveform h). This output pulse triggers the reset generator to produce a 350 microsecond reset pulse (waveform k) at tag A of the XK/A unit.

96. After approximately 18 milliseconds, the reset-delay generator resets to its stable state and removes the inhibit from the 'or' gate. Conditions now are such that one complete cycle of counting and display operations have been completed and the instrument will recommence a further cycle of counting and display operations.

97. When the Function switch is in the FREQUENCY X1 or X0.1 positions the gate times are 1 second or 10 seconds respectively.

Period Measurement (Fig. 26)

98. The waveforms for period measurement are shown with the Function switch (SB) in the PERIOD 1 position.

99. A typical signal input for period measurement is shown in waveform (a). Waveform (b) is the amplified and shaped output from the XB unit at tag C. At instant A a reset pulse has occurred (waveform K). The XD units are reset to 'decimal nine' and the 'or' gate is inhibited by the reset-delay generator pulse (waveform j).

100. At instant B the reset-delay generator reverts to its stable state to remove the inhibit from the 'or' gate. At the next output pulse from tag C of the XB unit (instant C), the control flip-flop is set to a state where the positive-going output will inhibit the bulbs and open the signal gate (waveform e) to permit the 10 microsecond pulses to have access to the totalizer chain (waveform g).

101. The second positive-going pulse at instant D from the XB unit (tag C) produces a negative-going output from the control flip-flop. This output 'closes' the signal gate (waveform e) to prevent the clock pulses reaching the totalizer chain.

102. The negative-going output, at instant D, from the control flip-flop is also applied to the display-time generator to set it to its quasi-stable state when a positive-going output pulse (waveform h) inhibits the 'or' gate. The bulb inhibit is also removed by the negative-going output pulse from the control flip-flop to permit the power amplifier VT1 to apply the negative supply to the display bulbs.

103. Toward the end of the display period, the display-time generator returns to its stable state (waveform h : instant A) to produce a positive-going output that triggers the reset-delay generator. The reset-delay generator produces a positive-going pulse that triggers the reset generator to produce a 350 microsecond reset pulse at tag A of the XK/A unit.

104. After approximately 18 milliseconds (waveform j), the reset-delay generator reverts to its stable state and at the same time removes the inhibit level from the 'or' gate. The instrument has completed one complete cycle and is in a condition to commence a further counting and display operation.

105. With the Function switch in the PERIOD 10, PERIOD 100 and PERIOD 1000 positions the gating pulses at tag C of the XB unit are applied via the 'or' gate to the XD units. 10, 100 or 1000 periods of the input signal are then counted.

External Operation (Fig. 27)

106. The waveforms for external operation are shown for double-line start-stop. The waveforms and description for single-line stop-start operation are similar, the only difference being that the STOP and START inputs are linked together on the instrument and the signal is applied to these and the black INPUT terminal.

107. A typical 'start' signal is shown in waveform (a); waveform (b) is a typical 'stop' signal. At instant A, a reset pulse has occurred (waveform j); the XD units are reset to 'decimal nine' and the 'or' gate is inhibited by the reset-delay generator pulse (waveform h).

108. At instant B the reset-delay generator reverts to its stable state to remove the inhibit level from the 'or' gate. With the 'start' pulse at instant C, the control flip-flop is set to a state where the positive-going output will inhibit the bulbs and 'open' the signal gate (waveform d) to provide access for the 1 millisecond pulses to the totalizer chain (waveform f).

109. The 'stop' pulse, at instant D, produces a negative-going pulse from the control flip-flop and is applied to the signal gate, the bulb inhibit and the display-time generator to have the following effects :-

(a) The signal gate 'closes' (waveform d) so that the 1 millisecond pulses are prevented from reaching the totalizer chain.

(b) Removes the bulb inhibit, to permit the power amplifier to apply the negative supply to the display bulbs.

(c) The display-time generator is triggered to produce a positive-going pulse that inhibits the 'or' gate.

110. When the RESET button is depressed to obtain a fresh display, the display-time generator returns to its stable state (waveform g : instant A) to provide a positive pulse that triggers the reset-delay generator. The reset-delay generator produces a positive-going pulse that triggers the reset generator, which produces the 350 microsecond system-resetting pulse at tag A of the XK/A unit.

111. After approximately 18 milliseconds (waveform h), the reset-delay generator reverts to its stable state and removes the inhibit from the 'or' gate so that a further counting and display operation can continue when the next 'start' pulse is received.

SECTION 2

MAINTENANCE

CONTENTS

CHAPTER 1

DISMANTLING AND RE-ASSEMBLY

CONTENTS

CHAPTER 1

DISMANTLING AND RE-ASSEMBLY

REMOVAL OF INSTRUMENT CASE

1. (1) Remove the two screws at the top of the wrap-round cover; these are near the front and rear of the handle.

(2) Remove the four screws at the bottom corners of the cover.

(3) Lift the cover off.

(4) Turn the instrument upside down with the panel furthest away.

(5) Loosen the two screws holding the front title strip and pull the title strip off.

(6) Remove the two 6 BA screws mounted between the third and fourth bank of ventilation holes.

(7) Remove the two right-hand feet (i. e. feet nearest front and rear controls).

(8) Lift the bottom cover off.

(9) Re-fitting of the instrument case is the reverse of the removal.

FUSES AND VOLTAGE SELECTOR PANEL

2. The fuses and voltage selector panels are located at the upper right-hand side of the instrument on a sub-chassis. The fuse rating is 1 amp. for the 200 to 240-volt ranges and 2 amp. for the 115-volt range.

REMOVAL OF A PRINTED WIRING BOARD

3. (1) Remove the case and base plate.

(2) With the instrument upside down on a bench, remove the two securing screws and washers which hold the channelled retaining bar.

(3) Unsolder the flying leads to the tags of the board to be removed, and note their respective positions.

(4) Cut the 20 s.w.g. tinned copper connecting links to the board.

(5) Lift the board clear.

(6) The fitting of a board is the reverse procedure to the removal.

(7) Replace with new lengths the tinned copper wire cut in operation (4). The inter-board wiring is shown in figure 32.

REPLACEMENT OF DISPLAY BULBS

4. (1) Remove the two screws and washers on the underside of the instrument which retain the title strip.

(2) Remove the display escutcheon which is held by a screw at each corner.

(3) Ease off the plastic moulded strips to expose the display bulbs.

(4) Unsolder and replace the faulty wired-in bulb. Spare bulbs are held in recesses in the plastic moulded strips. Great care should be taken when refitting the moulded strips to ensure that all the bulbs are aligned so that they engage with their respective holes, rather than being pushed back. Take care to ensure that no solder or pieces of wire drop into the instrument.

(5 (5) Re-assembly of the display escutcheon and title strip is the reverse of removal.

CHAPTER 2

CALIBRATION

CONTENTS

CHAPTER 2

CALIBRATION

INTRODUCTION

1. The instrument is accurately set-up after manufacture and should, under normal operational use, maintain its accuracy over a long period of time. Should it fail to give the expected display during operation or instrument check (Section 1, Chapter 2, paragraph 6) the following procedure should be carried out.

WARNING : This procedure should only be carried out by competent personnel with suitable test equipment after all other causes of error have been eliminated. If the necessary test equipment is not available, the instrument should be returned to the manufacturer.

2. The location of the preset controls that are adjusted during the alignment procedure is shown in Figure 34.

TEST EQUIPMENT

3. (a) Multi-range test meter e.g. Avo Model 8.

(b) An oscilloscope with an accurately calibrated time base, capable of measuring pulse widths to $\pm 3\%$.

(c) A digital frequency meter measuring up to 1 Mc/s with an accuracy of at least 1 part in 10^6.

OR

(d) A 200 kc/s Droitwich receiver together with an oscilloscope, preferably with one or other of the following features :-

(i) A double beam.

(ii) A Z-MOD input.

PRELIMINARY SETTING-UP

4. (1) Remove the wrap round top and side cover, and the base plate as described in Chapter 1, paragraph 1.

(2) Check that the voltage selector is correctly set for the mains voltage supply. (Section 1, Chapter 2, paragraphs 1 and 2.)

(3) Connect the instrument to the mains supply, and set the Function switch to one of the Frequency positions.

(4) Set the Count switch to the Test position.

(5) Check that the voltage outputs of the power supply on the printed wiring board tags M and L are nominally +12 volts and -12 volts respectively, and that tag E on XK/A board is -15 volts. All voltages are measured with respect to the 0-volt line which is tag B on all the boards.

1 Mc/s CRYSTAL OSCILLATOR ADJUSTMENT

5. A digital frequency meter with an accuracy of at least 1 part in 10^6 or an oscilloscope together with a frequency standard of better than 1 part in 10^6 stability are essential. A choice of four methods is given, one utilizing a digital frequency meter and three using a frequency standard with different types of oscilloscope. It is assumed that the user will have to resort to the Droitwich transmission of 200 kc/s as a frequency standard. The visual result obtained with the last three methods differs, and in order to check the stability, the oscilloscope trace must be observed for a period of at least 5 seconds, and the particular instructions for each method should be carried out.

NOTE : The adjustment to be described in paragraphs 6 to 10 should not be carried out until the instrument has been switched on for at least 30 minutes in an ambient temperature between 20° and 25°C to allow the oven and crystal temperature to become stabilized.

6. Method 1 : A digital frequency meter with an accuracy of at least 1 part in 10^6 is used.

(1) Connect the input terminals of the digital frequency meter to tag C of the XJ board; an earth is available at tag B.

(2) Adjust the variable capacitor CV1 (fig. 32) until the frequency meter indicates exactly 1 Mc/s.

7. Method 2 : A double-beam oscilloscope with an external trigger input is used.

(1) Connect the 200 kc/s output from the Droitwich receiver to the Y1 input terminal of the oscilloscope and also to the trigger input.

(2) Select a timebase speed which produces approximately two cycles over the trace length.

(3) Connect the 1 Mc/s oscillator output at tag C of the XJ board to the Y2 terminal of the oscilloscope; an earth point is available at tag B.

(4) Adjust the variable capacitor CV1 (fig. 32) until five cycles of the Y2 trace are stationary with respect to one cycle of the Y1 trace.

(5) Check that the Y2 trace does not drift by more than 1 cycle over a period of at least 5 seconds.

8. Method 3 : A single-beam oscilloscope with Z-MOD input is used.

(1) Switch off the oscilloscope timebase.

(2) Connect the 200 kc/s output from the Droitwich receiver to the oscilloscope Y - amplifier input.

(3) Connect the 1 Mc/s oscillator output tag C on the XJ board to the Z-MOD input of the oscilloscope; an earth point is available at tag B.

(4) The c.r.t. display will be a vertical trace superimposed with moving "bright up" spots.

(5) Adjust the variable capacitor CV1 (fig. 32) until the spots are stationary.

(6) Check that a "spot" does not move by more than the distance between two consecutive "spots" over a period of at least 5 seconds.

9. Method 4 : A simple single-beam oscilloscope with X and Y amplifiers is used.

(1) Switch off oscilloscope timebase.

(2) Connect the 200 kc/s output of the Droitwich receiver to the oscilloscope X - amplifier input.

(3) Connect the 1 Mc/s oscillator output at tag C on the XJ board to the oscilloscope Y - amplifier; an earth point is available at tag B.

(4) A moving Lissajous figure will be displayed on the oscilloscope c.r.t.

(5) Adjust the variable capacitor CV1 (fig. 32) until the Lissajous figure becomes stationary.

(6) Check that the Lissajous figure does not re-cycle more than once during a period of at least 5 seconds.

SYNCHRONOUS DIVIDERS

10. An oscilloscope with an accurately calibrated timebase capable of measuring pulse widths to ±3% is required for checking and setting-up the synchronous dividers.

(1) Connect the Y input terminals of the oscilloscope to tags J and B (earth) of the XJ unit.

(2) Adjust the variable resistor RV1, on the XJ unit (fig. 34), until the period of the waveform is 10 microseconds (rather than 9 or 11 microseconds).

(3) Further adjust RV1 until the width of the pulse displayed is exactly 1 microsecond at half pulse height.

(4) Transfer the Y input terminals to tags J and B (earth) of the XH unit.

(5) Adjust the variable resistor RV1, on the XH unit (fig. 34), until the period of the waveform is 100 microseconds (rather than 90 or 110 microseconds).

(6) Further adjust RV1 until the width of the pulse displayed is exactly 5.5 microseconds at half pulse height.

(7) Transfer the Y input terminal from tag J to tag K of the XH unit.

(8) Adjust the variable resistor RV2 (fig. 34) until the period of the waveform is 1 millisecond (rather than 0.9 or 1.1 milliseconds).

(9) Further adjust RV2 until the width of the pulse displayed is exactly 70 microseconds at half pulse height.

(10) Transfer the Y input terminal from tag K to tag D on the XH unit.

(11) Adjust the variable resistor RV3 (fig. 34) until the period of the waveform is 10 milliseconds (rather than 9 or 11 milliseconds).

(12) Further adjust RV3 until the width of the pulse displayed is exactly 700 microseconds at half pulse height.

(13) Connect the Y input terminals of the oscilloscope to tags H and J in turn (tag B common earth) of the XJ unit and check that a frequency division ratio of ten occurs between J and H.

(14) Connect the Y input terminals of the oscilloscope to tag J of the XJ unit and tag J of the XH unit in turn (tag B: earth) and check that a frequency division ratio of ten occurs between tag J of the XH unit and tag J of the XJ unit.

(15) Connect the Y input terminals of the oscilloscope to tags J, K and D in turn (tag B common earth) of the XH unit, and check that a frequency division of ten occurs between K and J, D and K respectively.

AMPLIFIER GAIN

11. (1) Switch the AC/DC switch to DC and apply a 100 kc/s, 3 V r.m.s. signal to the input terminals.

(2) Set the Function switch to FREQUENCY X10.

(3) Monitor the output at pin F on the XB unit with an oscilloscope.

(4) Adjust RV1 on the XB unit until the 'blips' on the waveform (fig. 19 : waveform C) are equi-distant about the mean level.